## AK1221 3500MHz High Lineartity Mixer

## 1. Overview

The AK1221 is high linearity mixer. RF and Lo frequency range coverage is from 700 to 3500 MHz and IF coverage is from 20 to 1000 MHz . The RF input provides single-ended $50 \Omega$ interface. Lo ports are $50 \Omega$ matched and complementary input should be decoupled to the ground. IF output ports are differential open drain outputs. The linearity and power consumption performances can be optimized by the resistance connected to the BIAS Pin.

## 2. Features

$\square$ Operating Frequency: $\quad 700 \mathrm{MHz}$ to 3500 MHz
$\square \quad$ Linearity vs. Power selectable architecture
Power Consumption: 45mA, IIP3: +25dBm, Gain: -0.5dB, NF: 14dB
$\square \quad$ Lo input level:
$0 \mathrm{dBm} \pm 5 \mathrm{~dB}$
ㅁ Operating Supply Voltage:
4.75 to 5.25 V
$\square \quad$ Package: $\quad 16$ pin UQFN $(0.5 \mathrm{~mm}$ pitch, $3 \mathrm{~mm} \times 3 \mathrm{~mm} \times 0.60 \mathrm{~mm})$
$\square$ Operating Temperature Range:
-40 to $85^{\circ} \mathrm{C}$

## 3. Applications

- Cellular BTS / Repeater
$\square \quad$ Two-way Radios (PMR/LMR)


## 4. Table contents

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## 5. Block Diagram



Figure 1. Block Diagram

## 6. System Diagram



Figure 2. System Diagram

## 7. Pin Functional Description

Table 1 Pin Function

| No. | Name | I/O | Pin Functions | Remarks |
| :---: | :---: | :---: | :--- | :--- |
| 1 | RFIN | AI | RF Input | Connecting an inductor between this pin and ground. |
| 2 | VSS | G | Ground pin |  |
| 3 | VSS | G | Ground pin |  |
| 4 | LOINN | AI | Lo Input Negative |  |
| 5 | LOINP | AI | Lo Input Positive |  |
| 6 | VDD | P | Power Supply |  |
| 7 | VDD | P | Power Supply |  |
| 8 | VDD | P | Power Supply | This pin is open drain output. |
| 9 | VDD | P | Power Supply | It needs power feeding via an inductor. |
| 10 | BIAS | AIO | Resistance pin for current | Connecting a resistor between this pin and ground. |
| 11 | IFOUTN | AO | IF Output Negative | This pin is open drain output. |
| 12 | IFOUTP | AO | IF Output Positive |  |
| 13 | VSS | G | Ground pin |  |
| 14 | VSS | G | Ground pin |  |
| 15 | VSS | G | Ground pin | Ground pin |
| 16 | VSS | G | Greeding via an inductor. |  |

Note) The exposed pad at the center of the backside should be connected to ground.

| $\mathrm{AI}:$ Analog input pin | AO : Analog output pin | AIO : Analog I/O pin |
| :--- | :--- | :--- |
| $\mathrm{P}:$ Power supply pin | $\mathrm{G}:$ Ground pin |  |
|  |  |  |



Figure 3. Package Pin Layout

## 8. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit | Remarks |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Supply Voltage | VDD | -0.3 | 5.5 | V |  |
| RF Input Power | RFPOW |  | 12 | dBm |  |
| LO Input Power | LOPOW |  | 12 | dBm |  |
| Storage Temperature | Tstg | -55 | 125 | ${ }^{\circ} \mathrm{C}$ |  |

Exceeding these maximum ratings may result in damage to the AK1221. Normal operation is not guaranteed at these extremes.

## 9. Recommended Operating Range

Table 3 Recommended Operating Range

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remarks |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Operating <br> Temperature | Ta | -40 |  | 85 | ${ }^{\circ} \mathrm{C}$ |  |
| Supply Voltage | VDD | 4.75 | 5 | 5.25 | V |  |

The specifications are applicable within the recommended operating range (supply voltage/operating temperature).

## 10. Electrical Characteristics

## 1. Analog Circuit Characteristics

Unless otherwise noted IF output $=150 \mathrm{MHz}$, Lo Input Level $=-5 \mathrm{dBm}$ to +5 dBm , Output Load Resistor (RLoad) $=680 \Omega$, VDD $=4.75$ to 5.25 V , $\mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$

| Parameter |  | Min. | Typ. | Max. | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RF Input Frequency |  | 700 |  | 3500 | MHz |  |
| Lo Input Frequency |  | 700 |  | 3500 | MHz |  |
| IF output Frequency |  | 20 |  | 1000 | MHz |  |
| Lo Input Power |  | -5 | 0 | +5 | dBm |  |
| Current Adjustment Resistor(BIAS) |  | 22 |  | 56 | k $\Omega$ |  |
| IDD | BIAS $=22 \mathrm{k} \Omega$ |  | 64 | 87 | mA | The total current of VDD pin, IFOUTP pin and IFOUTN pin. |
|  | BIAS $=33 \mathrm{k} \Omega$ |  | 45 | 64 | mA |  |
|  | BIAS $=56 \mathrm{k} \Omega$ |  | 30 | 44 | mA |  |
| RFIN= $\mathbf{2 5 0 0 M H z}$, Current Adjustment Resistor $=33 \mathrm{k} \Omega$ |  |  |  |  |  |  |
| Conversion Gain |  | -2.5 | -0.5 | 1.5 | dB |  |
| SSB Noise Figure |  |  | 14 | 16.5 | dB | Design guarantee value |
| IP1dB |  | 7 | 10 |  | dBm |  |
| IIP3 |  | 21 | 25 |  | dBm | Design guarantee value |

## 11. Typical Performance

Unless otherwise noted, RF input $=2500 \mathrm{MHz}$, Lo input $=2350 \mathrm{MHz}$, IF output $=150 \mathrm{MHz}$, Output Load Resistor (RLoad) $=680 \Omega$

## 1. Current Adjustment Resistor vs. IIP, NF, P1dB, Gain, IDD







Figure 4. Current Adjustment Resistor vs. IIP3, NF, P1dB, Gain, IDD
Note ) A resistor with 5\% tolerance are used.
2. Over temperature vs. IIP3, NF, P1dB, Gain, IDD


Figure 5. Over temperature vs. IIP3, NF, IP1dB, Gain, IDD
3. Supply voltage vs. IIP3, NF, P1dB, Gain, IDD






Resistance for current adjustment
_

$=$| 22kohm |
| :--- |
| $33 k o h m$ |
| $56 k o h m$ |

Figure 6. Supply voltage vs. IIP3, NF, IP1dB, Gain, IDD
4. RF input frequency vs. IIP3, NF, Gain





Resistance for current adjustment


Figure 7. RF input frequency vs. IIP3, NF, Gain
5. IF input frequency vs. IIP3, NF, Gain


Resistance for current adjustment
_

$=$| 22kohm |
| :--- |
| 33kohm |
| $56 k o h m$ |

$=-=\quad$

Figure 8. IF input frequency vs. IIP3, NF, Gain
6. Lo input power vs. IIP3, NF, Gain





Resistance for current adjustment


Figure 9. Lo input power vs. IIP3, NF, Gain
7. Output Load Resistor (RLoad) vs. IIP3, NF, Gain





Resistance for current adjustment
_

$=$| 22kohm |
| :--- |
| $33 k o h m$ |

$-=-\quad$
$56 k o h m$

Figure 10. Output Load Resistor(RLoad) vs. IIP3, NF, Gain

## 8. Leakage

RFIN $=2500 \mathrm{MHz},-20 \mathrm{dBm}$, LO input $=2350 \mathrm{MHz}, 0 \mathrm{dBm}$, RLoad= $=680 \Omega, \mathrm{Ta}=25^{\circ} \mathrm{C}$ VDD $=5 \mathrm{~V}$

| Parameter | BIAS | Typ. | Unit |
| :--- | :--- | :--- | :--- |
| RF - LO Leakage | $22 \mathrm{k} \Omega$ | -36 | dBc |
|  | $56 \mathrm{k} \Omega$ | -36 | dBc |
| RF - IF Leakage | $22 \mathrm{k} \Omega$ | -61 | dBc |
|  | $56 \mathrm{k} \Omega$ | -57 | dBc |
| LO - RF Leakage | $22 \mathrm{k} \Omega$ | -44 | dBc |
|  | $56 \mathrm{k} \Omega$ | -44 | dBc |
|  | $22 \mathrm{k} \Omega$ | -58 | dBc |
|  | $56 \mathrm{k} \Omega$ | -66 | dBc |

## 12. Typical Evaluation Board Schematic

1. Typical Evaluation Board Schematic


Figure 11. Typical Evaluation Board Schematic

Note 1) The open drain output needs power feeding via a inductor. (IFOUTP pin and IFOUTN pin)
Note 2) It is necessary to adjust impedance matching as to its setting frequency. (RF input and IF output)
2. Example of impedance matching

2-1 RFIN
RF Input


| Frequency[MHz] | C1[pF] | C2[pF] | $\mathrm{L} 1[\mathrm{nH}]$ | L2[nH] | Impedance[ohm] |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 700 | none | 20 | none | 39 | $42.9-\mathrm{j} 5.4$ |
| 2500 | 39 | 2.2 | 1.8 | 10 | $61.2-\mathrm{j} 12.8$ |
| 3500 | 39 | 1.0 | 1.0 | 10 | $40.7-\mathrm{j} 5.1$ |

## 2-2 IFOUT



| Frequency [MHz] | R1 [ohm] | C1 [pF] | $\mathrm{C} 2[\mathrm{pF}]$ | L1 [ nH ] | L2 [ nH ] | Impedance[ohm] |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 20 | 680 | 15 | none | $1200{ }^{* 1}$ | $1200{ }^{* 1}$ | 56.6 - j4.5 |
| 150 | 680 | 1 | None | 180 *2 | $180{ }^{\text {*2 }}$ | $52.6+\mathrm{j} 1.6$ |
| 200 | 680 | none | none | 150 *2 | 150 *2 | 47.0-j11.9 |
| 500 | 440 | 0.2 | 1.8 | $43{ }^{* 2}$ | $43{ }^{* 2}$ | 49.2 - j2.3 |
| 750 | 440 | 0.3 | 1.3 | $20{ }^{*}$ | $20{ }^{\text {*2 }}$ | $51.7+$ j3.4 |
| 1000 | 440 | 0.1 | 1.2 | $12^{* 2}$ | $12^{* 2}$ | 53.2 - j4.9 |

*1)Murata LQW21A series
*2)Murata LQW18A series

## 2 - 3 LOINP/LOINN


13. LSI Interface Schematic

| No. | Name | I/O | Function |
| :---: | :---: | :---: | :---: |
| 1 | RFIN | 1 | RF Input pin |
| 4 | LOINN | 1 | Lo Input pins |
| 5 | LOINP |  |  |
| 10 | BIAS | I/O | Analog I/O pin |
| 11 | IFOUTN | O | IF Output pins |
| 12 | IFOUTP |  |  |

## -Impedance matching network with LC



Figure 12. Impedance matching network with LC

Impedance matching network with LC is shown in Figure 12. AK1221 has open drain outputs, so RL1 + RL2 is output load resistance. C11 and L11 compose lowpass filter. C12 and L12 are for highpass filter. C13 is DC blocking capacitor and L13 is RF choke. IFOUTP and IFOUTN pins need power feeding via L11, L12 and L13.

The differential voltage from IFOUTP/N can be converted to a single-ended by L11, L12, C11 and C12 properly. The differential impedance (RL1 + RL2) is converted to single-ended output terminating impedance Ro.

L11, C11, L12 and C12 are calculated as below. fout is IF output frequency.
$C_{11}=C_{12}=\frac{1}{2 \pi * f_{\mathrm{OUT}} * \sqrt{\left(R_{\mathrm{L} 1}+R_{\mathrm{L} 2}\right) * R_{\mathrm{O}}}}$
$L_{11}=L_{12}=\frac{\sqrt{\left(R_{\mathrm{L} 1}+R_{\mathrm{L} 2}\right) * R_{\mathrm{O}}}}{2 \pi^{*} f_{\mathrm{OUT}}}$

For example, in the case of IF Output $=50 \mathrm{MHz}$, Output Load Resistor (Rload) $=660 \Omega$ in $50 \Omega$ interface, L11, C11, L12 and C12 are calculated as below.
$C_{11}=C_{12}=\frac{1}{2 \pi *\left(150 * 10^{\wedge} 6\right) * \sqrt{660 * 50}}=5.84 \mathrm{pF}$
$L_{11}=L_{12}=\frac{\sqrt{660 * 50}}{2 \pi *\left(150 * 10^{\wedge} 6\right)}=193 \mathrm{nH}$

L13 and C13 should be large enough not to affect the impedance at IF output frequency. In some cases the impedance matching can be optimized by L13 and C13.

For example, in the case of IF Output $=150 \mathrm{MHz}$, Output Load Resistor (Rload) $=660 \Omega$ in $50 \Omega$ interface, it is recommended to choose 2200 nH and 1000 pF as L13 and C13. If any correction is needed, it can be adjusted by reducing the value of L13 and C13.

In some cases L14 can be selected to resonate with IF output capacitance. The typical differential output impedances for several frequencies are below. In the case of IF Output $=150 \mathrm{MHz}$, it is recommended to choose 1000 nH as L14.

|  | Differential Output Impedance |  | Matching Element |
| :---: | :---: | :---: | :---: |
| IF Output Frequency [MHz] | R[ohm] | $j$ X[ohm] | L14 [nH] |
| 20 | 2300 | $-J 4083$ | OPEN |
| 50 | 711 | $-J 2448$ | OPEN |
| 70 | 419 | $-J 1873$ | OPEN |
| 100 | 244 | $-J 1420$ | 2200 |
| 150 | 109 | - J932 | 1000 |
| 180 | 77 | $-J 788$ | 750 |
| 200 | 62 | - J706 | 560 |
| 250 | 38 | $-J 566$ | 360 |
| 300 | 28 | - J470 | 240 |
| 400 | 16 | $-J 346$ | 150 |
| 500 | 15 | $-J 270$ | 82 |
| 600 | 13 | $-J 223$ | 62 |
| 700 | 10 | $-J 188$ | 43 |
| 800 | 9 | - J159 | 33 |
| 900 | 7 | $-J 138$ | 24 |
|  |  |  |  |

These calculated values are approximation. In some cases, some correction is needed due to the effect of parasitic capacitance of external parts or/and PCBs. The impedance matching network components should be decided through enough evaluation on AK1221.

Typical Performance using impedance matching network with LC is below. RF Input $=2500 \mathrm{MHz}$, IF Output $=$ 150 MHz , LO Input $=2350 \mathrm{MHz}$, Output Load Resistor (Rload) $=660 \Omega$, Vdd $=5 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}$, LO Input Level $=$ OdBm, current adjustment resistor $=33 \mathrm{k} \Omega$.

| Ref. | Value | Size | Part Number |
| :--- | :--- | :--- | :--- |
| RL1, RL2 | $330 \Omega$ | 1005 | KOA RK73B1ETTP331 |
| L11, L12 | 200 nH | 1608 | Murata LQW18ANR20G00 |
| C11, C12 | 6 pF | 1005 | Murata GJM1552C1H6R0DB01 |
| L13 | 2200 nH | 2012 | Murata LQW21HN2R2J00 |
| C13 | 1000 pF | 1005 | Murata GRM1552C1H102JA01 |
| L14 | 1000 nH | 2012 | Murata LQW21HN1R0J00 |


| Parameter | Min. Typ. Max. | Unit |
| :--- | :---: | :---: |
| Conversion Gain | -1.1 | dB |
| SSB Noise Figure (NF) | 13.8 | dB |
| IP1dB | 11.6 | dBm |
| IIP3 | 24.8 | dBm |

The phase and amplitude balance is achieved at IF Output frequency by using impedance matching network with LC. The port-to-port leakage is improved with the phase and amplitude balance is achieved at RF, LO, and IF frequency with wide band balun.

## - Evaluation Board



Figure 13. AK1221 Evaluation Board (Balun)


Figure 14. AK1221 Evaluation Board Schematic (Balun)


Figure 15. AK1221 Evaluation Board (matching network with LC)


Figure 16. AK1221 Evaluation Board Schematic (matching network with LC)

## 15. Outer Dimensions


$\%$
$\infty$
+1
$\infty$
1
0
0




Figure 17. Outer Dimensions

Note 1.1 pin marking is only a reference for the 1 pin location on the top of package.

## 16. Marking

(a) Style

UQFN
(b) Number of pins
(c) 1 pin marking: -
(d) Product number 1221
(e) Date code

Y: Lower 1 digit of calendar year (Year $2012 \rightarrow 2,2013 \rightarrow 3 \ldots$ )
WW: Week
L: Lot identification, given to each product lot which is made in a week $\rightarrow$ LOT ID is given in alphabetical order (A, B, C...).


Figure 18. Marking

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## AsahiKASEI

-Related Parts

| Part\# | Discription | Comments |
| :---: | :---: | :---: |
| Mixer |  |  |
| AK1220 | 100MHz 900MHz High Linearity Down Conversion Mixer | IIP3:+22dBm |
| AK1222 | 100MHz~900MHz Low Power Down Conversion Mixer | IDD:2.9mA |
| AK1224 | 100MHz 900MHz Low Noise, High Liniarity Down Conversion Mixer | NF:8.5dB, IIP3:+18dBm |
| AK1228 | 10MHz 2 GHz Up/Down Conversion Mixer | 3V Supply, NF:8.5dB |
| AK1221 | $0.7 \mathrm{GHz} \sim 3.5 \mathrm{GHz}$ High Linearity Down Conversion Mixer | IIP3:+25dBm |
| AK1223 | 3GHz~8.5GHz High Linearity Down Conversion Mixer | IIP3:+13dB, NF:15dB |
| PLL Synthesizer |  |  |
| AK1541 | 20MHz~600MHz Low Power Fractional-N Synthesizer | IDD: 4.6 mA |
| AK1542A | $20 \mathrm{MHz} \sim 600 \mathrm{MHz}$ Low Power Integer-N Synthesizer | IDD: 2.2 mA |
| AK1543 | $400 \mathrm{MHz} \sim 1.3 \mathrm{GHz}$ Low Power Fractional-N Synthesizer | IDD: 5.1 mA |
| AK1544 | $400 \mathrm{MHz} \sim 1.3 \mathrm{GHz}$ Low Power Integer-N Synthesizer | IDD: 2.8 mA |
| AK1590 | $60 \mathrm{MHz} \sim 1 \mathrm{GHz}$ Fractional-N Synthesizer | IDD: 2.5 mA |
| AK1545 | $0.5 \mathrm{GHz} \sim 3.5 \mathrm{GHz}$ Integer-N Synthesizer | 16-TSSOP |
| AK1546 | $0.5 \mathrm{GHz} \sim 3 \mathrm{GHz}$ Low Phase Noise Integer-N Synthesizer | Normalized C/N:-226dBc/Hz |
| AK1547 | $0.5 \mathrm{GHz} \sim 4 \mathrm{GHz}$ Integer-N Synthesizer | 5V Supply |
| AK1548 | $1 \mathrm{GHz} \sim 8 \mathrm{GHz}$ Low Phase Noise Integer-N Synthesizer | Normalized C/N:-226dBc/Hz |
| IFVGA |  |  |
| AK1291 | 100~300MHz Analog Signal Control IF VGA w/ RSSI | Dynamic Range:30dB |
| integrated VCO |  |  |
| AK1572 | $690 \mathrm{MHz} \sim 4 \mathrm{GHz}$ Down Conversion Mixer with Frac.-N PLL and VCO | IIP3:24dBm, -111dBc/Hz@100kHz |
| AK1575 | $690 \mathrm{MHz} \sim 4 \mathrm{GHz}$ Up Conversion Mixer with Frac.-N PLL and VCO | IIP3:24dBm, -111dBc/Hz@100kHz |
| IF Reciever (2nd Mixer + IF BPF + FM Detector) |  |  |
| AK2364 | Built-in programmable AGC+BPF, FM detector IC | IFBPF: $\pm 10 \mathrm{kHz} \sim \pm 4.5 \mathrm{kHz}$ |
| AK2365A | Built-in programmable AGC+BPF, IFIC | IFBPF: $\pm 7.5 \mathrm{kHz} \sim \pm 2 \mathrm{kHz}$ |
| Analog BB for PMR/LMR |  |  |
| AK2345C | CTCSS Filter, Encoder, Decoder | 24-VSOP |
| $\begin{aligned} & \hline \text { AK2360/ } \\ & \text { AK2360A } \end{aligned}$ | Inverted frequency( $3.376 \mathrm{kHz} / 3.020 \mathrm{kHz}$ ) scrambler | 8-SON |
| AK2363 | MSK Modem/DTMF Receiver | 24-QFN |
| AK2346B | 0.3-2.55/3.0kHz Analog audio filter, | 24-VSOP |
| AK2346A | Emphasis, Compandor, scrambler, MSK Modem | 24-QFN |
| AK2347B | 0.3-2.55/3.0kHz Analog audio filter | 24-VSOP |
| AK2347A | Emphasis, Compandor, scrambler, CTCSS filter | 24-QFN |
| Function IC |  |  |
| AK2330 | 8-bit 8ch Electronic Volume | VREF can be selected for each channel |
| AK2331 | 8-bit 4ch Electronic Volume | VREF can be selected for each channel |

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