PIC16HV540

PIC16HV540 Data Sheet Errata

The PIC16HV540 parts you have received conform functionally to the Device Data Sheet (DS40197**B**), except for the anomalies described below.

None.

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Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40197**B**), the following clarifications and corrections should be noted.

1. Module: PORTB

1. Page 19, Section 5.2 **PORTB** of DS40197B has an error in the text. The Text reads: Only pins configured as inputs can cause this wake-up on pin change to occur.

The corrected text should read: Only pins **RB<0:3> when** configured as inputs can cause this wake-up on pin change to occur.

Note:	RB7 will always wake-up the device if driven to a logic 1 during SLEEP mode. This will happen if RB7 is configured as an input or output.

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2. Module: DC Characteristics

Table 10.1, Regulation Voltage, Max. changes from 6 to 6.5, as shown in bold below.

TABLE 10-1: DC CHARACTERISTICS: PIC16HV540-04, 20 (COMMERCIAL) PIC16HV540-04I, 20I (INDUSTRIAL)

DC Characteristics Power Supply Pins		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym.**	**Min.**	**Typ(1)**	**Max.**	**Units**	**Conditions**
Supply Voltage	VDD	3.5 4.5	 —	15 15	V V	LP, XT and RC modes HS mode
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See section on Power-on Reset for details
VDD rise rate to ensure Power-on Reset	SVDD	0.05 VDD			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) HS option XT and RC(4) options LP option	IDD	 — — —	 5 1.8 300	 20 3.3 500	 mA mA µA	 FOSC = 20 MHz, VDD = 15V, VREG = 5V FOSC = 4 MHz, VDD = 15V, VREG = 5V FOSC = 32 kHz, VDD = 15V, VREG = 5V, WDT disabled
Power-down Current(5)(6)	IPD	 — — — —	 4.5 0.25 1.8 1.4	 20 14 10 5	 µA µA µA µA	 VDD = 15V, VREG = 5V SLEEP timer enable, BOD disabled VDD = 15V, VREG = 3V SLEEP timer enable, BOD disabled VDD = 15V, VREG = 5V SLEEP timer disabled, BOD disabled VDD = 15V, VREG = 3V SLEEP timer disabled, BOD disabled
Brown-out Current		—	0.5	—	µA	VDD = 15V, VREG = 5V, BOD enabled
Brown-out Detector Threshold	BVDD	2.7 1.8	3.1 2.2	4.2 2.8	V V	VDD = 15V, VREG = 5V* (7) VDD = 15V, VREG = 3V* (7)
Regulation Voltage	VIO	2 4	3 5	4.5 **6.5**	V V	VDD = 15V, VREG = 3V, Unloaded outputs, SLEEP VDD = 15V, VREG = 5V, Unloaded outputs, SLEEP

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

6: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection, if the SLEEP mode is exited or during initial power-up.

7: See Section 7.6.1 for additional information.

REVISION HISTORY

Rev A Document (6/2003)
Added Item 2 to the Clarification/Corrections to the Data Sheet Section, changing max. of Regulation Voltage from 6 to 6.5.

Rev B Document (6/2003)
Previous errata, DS80123A was combined with this errata. Error in text, Section 5.2, PORTB of the data sheet.

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