## ADP1046A Evaluation Board User Guide

## Wide Input Range, Full Bridge Phase Shifted Topology using the ADP1046A

## FEATURES

600 W phase shifted full bridge topology Wide input range to minimize hold up capacitor Wide ZVS range down to $\mathbf{1 0 \%}$ rated load Short-circuit and fast overvoltage protection
Remote voltage sensing
Line voltage feedforward
$I^{2} \mathrm{C}$ serial interface to PC
Software GUI
Programmable digital filters for DCM and CCM
7 PWM outputs including auxiliary PWM Digital trimming
Current, voltage, and temperature sense through GUI Calibration and trimming

## CAUTION

This evaluation board uses high voltages and currents. Extreme caution must be taken, especially on the primary side, to ensure safety for the user. It is strongly advised to power down the evaluation board when not in use. A current-limited power supply is recommended.

## ADP1046A EVALUATION BOARD OVERVIEW

This evaluation board features the ADP1046A in a switching power supply application. With the evaluation board and software, the ADP1046A can be interfaced to any PC running Windows ${ }^{\star}$ 2000, Windows XP, Windows Vista, Windows NT, or Windows 7 via the USB port of the PC. The software allows control and monitoring of the ADP1046A internal registers.
The evaluation board is set up for the ADP1046A to act as an isolated switching power supply with a rated load of $48 \mathrm{~V} / 12.5 \mathrm{~A}$ from an input voltage ranging from 340 V dc to 410 V dc.

## ADP1046A EVALUATION BOARD PHOTOGRAPH



Figure 1.

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## REVISION HISTORY

## 10/14—Revision 0: Initial Version

## BOARD SPECIFICATIONS

Table 1. Target Specifications

| Specification | Min | Typ | Max | Unit | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IN }}$ | 340 | 385 | 410 | V |  |
| Vout |  | 48 |  | V |  |
| lout | 0.0 | 12.5 | 15 | A | With 400 LFM air flow |
| Overload Current (OCP Limit) |  |  | 15 | A | OCP set to shut down PSU after $\sim 10 \mathrm{~ms}$ |
| Efficiency |  | 96.35 |  | \% | Typical reading at $385 \mathrm{~V} 1{ }^{\text {IN }}, 12.5 \mathrm{~A}$ load |
| Switching Frequency |  | 111.6 |  | kHz |  |
| Output Voltage Ripple |  | 550 |  | mV | At 12.5 A load |

## TOPOLOGY AND CIRCUIT DESCRIPTION

This evaluation board circuit consists of the ADP1046A in a typical isolated dc-to-dc switching power supply in a full bridge phase shifted topology with synchronous rectification. The circuit provides a rated output load of $48 \mathrm{~V} / 12.5 \mathrm{~A}$ from a nominal input voltage of 385 V dc operated in continuous conduction mode (CCM) at all times. The ADP1046A provides functions such as output voltage regulation, output overvoltage protection, input and output current protection, primary cycle by cycle protection, and overtemperature protection. Figure 70 provides a top level schematic that describes the power flow and auxiliary power supply that starts up at 50 V dc and provides power to the ADP1046A through a 3.3 V low dropout regulator (LDO), the $i$ Coupler ${ }^{*}$ isolation plus gate drivers, the on-board fan, and the synchronous rectifier drivers. The auxiliary power supply using the transformer (T3) and IC (U10) generates a 12 V rail on the primary side and a 13 V rail on the secondary side. The main power transformer (T12) provides a wide input voltage range ( 340 V dc to 410 V dc ), and the circuit has a wide zero voltage switching (ZVS) range down to $10 \%$ of the rated load.
The primary side consists of the input terminals (JP8 and JP9), the switches (Q1 to Q4), the current sense transformer (T5), and the main transformer (T1). There is also a resonant inductor that aids in zero voltage switching at lighter load conditions. The ADP1046A is situated on the secondary side and is powered via the auxiliary power supply, or the USB connector via the LDO. The gate signal for the primary switches is generated by the ADP1046A through the $i$ Couplers and fed into the MOSFET drivers (U17 and U18). Bypass capacitors (C71, C72, and C114 to 116) are placed closed to the primary switches. Diodes (D36 and 37) clamp the resonance between the resonant inductor and the output capacitance (COSS) of the output rectifiers.
The secondary (isolated) side of the transformer consists of a center tapped winding. The synchronous rectifier driver (U7) provides the drive signals for the switches (Q9 and Q23). The output inductor (L8) and output capacitor (C11 and C41) act as a low-pass filter for the output voltage. The output voltage is fed back to the ADP1046A using a voltage divider and has a nominal
voltage of 1 V , which is differentially sensed. Output current is measured using a sense resistor (R2), which is also differentially sensed. To protect the synchronous rectifiers from exceeding the peak reverse voltage, an RCD clamp is implemented (D58, D59, R112 to R115, and C94).
The primary current is sensed through the CS1 pin with a small RC time constant ( R 44 and C22) that acts as a low-pass filter to remove the high frequency noise on the signal. An additional RC can be placed; however, the internal $\Sigma-\Delta$ analog-to-digital converter (ADC) naturally averages the signal. The position of the current transformer is placed in series with the resonant inductor to avoid saturation.
Line voltage feedforward is implemented using an RCD circuit (D13, R59, R64, C38, and C43) that detects the peak voltage at the synchronous field effect transistor (FET). There are two time constants that can be implemented in series with each other. The time constants must be matched such that it retains the peak value during the switching frequency period, but also is not too long in case there is a step down change in the input voltage. This peak voltage is further ratioed and fed in the ACSNS pin of the controller (ADP1046A). A thermistor (RT1) is placed on the secondary side close to the synchronous FET and acts as thermal protection for the power supply. A $16.5 \mathrm{k} \Omega$ resistor is placed in parallel with the thermistor that allows the software GUI to read the temperature directly in degrees Celsius.
Capacitor C69 is a YCAP that reduces common-mode noise from the transformer.
Also available on the secondary side is a 4-pin connector for $\mathrm{I}^{2} \mathrm{C}$ communication. This connector allows the PC software to communicate with the IC through the USB port of the PC. The user can easily change register settings on the ADP1046A and monitor the status registers. It is recommended that the USB dongle be connected directly to the PC, and not via the external hub.
Switch SW2 acts as a hardware PS_OFF switch. The polarity is configured using the GUI to be active high.

## CONNECTORS

Table 2 lists the connectors on the board. Table 3 lists the pinouts of the USB to $\mathrm{I}^{2} \mathrm{C}$ adapter, shown in Figure 2.

Table 2. Board Connectors

| Connector | Evaluation Board Function |
| :--- | :--- |
| J8 | DC input positive terminal |
| J9 | DC input negative terminal |
| J11 | Output voltage positive terminal |
| J12 | Output voltage negative terminal |
| J16 | Socket for auxiliary power supply |
| J18 | I$^{2}$ C connector |

Table 3. I ${ }^{2} \mathrm{C}$ Connector Pinout Descriptions

| Pin (Left to Right) | Function |
| :--- | :--- |
| 1 | 5 V |
| 2 | SCL |
| 3 | SDA |
| 4 | Ground |

Figure 2. ${ }^{1}$ C C Connector (Pin 1 on Left)


Figure 3. ADP1046A Evaluation Board (Side View)


Figure 4. Evaluation Board (Top View)

## SETTING FILES AND EEPROM

The ADP1046A communicates with the GUI software using the $\mathrm{I}^{2} \mathrm{C}$ bus.
The register settings (having the extension .46r) and the board settings (having the extension $\mathbf{. 4 6 b}$ ) are two files that are associated with the ADP1046A software. The register settings file contains information such as the overvoltage and overcurrent limits, the soft start timing, and the PWM settings that govern the functionality of the device. The ADP1046A stores all its settings in the EEPROM.

The EEPROM on the ADP1046A does not contain any information about the board, such as the current sense resistor, output inductor, and capacitor values. This information is stored in the board setup file (extension $\mathbf{. 4 6 b}$ ) and is necessary for the GUI to display the correct information in the Monitor tab as well as the Filter Settings window. The entire status of the power supply, such as the ORFET and synchronous rectifiers
enable/disable, primary current, output voltage, and current, can therefore be digitally monitored and controlled using the software only. Always make sure that the correct board file has been loaded for the board currently in use.
Each ADP1046A chip has trim registers for the temperature, the input current, the output voltage and current, and ACSNS. These values can be configured during production and are not overwritten when a new register settings file is loaded. Therefore, the trimming of all the ADCs for that corresponding environmental and circuit condition (such as component tolerances or thermal drift) are retained. A guided Auto Trim Wizard starts up, which trims the previously mentioned quantities so that the measurement value matches the values displayed in the GUI to allow ease of control through the software.


Figure 5. ADP1046A and GUI Interaction

## BOARD EVALUATION

## EQUIPMENT

The following equipment is required:

- A dc power supply ( 300 V to $400 \mathrm{~V}, 600 \mathrm{~W}$ )
- An electronic load ( $60 \mathrm{~V} / 600 \mathrm{~W}$ )
- An oscilloscope with differential probes
- A PC with ADP1046A GUI installed
- Precision digital voltmeters (HP34401or equivalent, 6 digits) for measuring dc current and voltage


## SETUP

Take the following steps to set up the evaluation board. Do not connect the USB cable to the evaluation board until the software has finished installing.

1. Install the ADP1046A software by inserting the installation CD. The software setup starts automatically, and a guided process installs the software as well as the USB drivers for communication between the GUI and the IC using the USB dongle.
2. Insert the daughter card in Connector J16 as shown in Figure 72.
3. Ensure that the PS_ON switch (SW1 on the schematic) is turned to the off position. The switch is located on the bottom left half of the board.
4. Connect one end of USB dongle to the board and the other end to the board to the USB port on the PC using the USB to $\mathrm{I}^{2} \mathrm{C}$ interface dongle.
5. The software reports that the ADP1046A has been located on the board. Click Finish to proceed to the main software interface window. The serial number reported on the side of the checkbox indicates the USB dongle serial number, as shown in Figure 6. The windows also displays the device $I^{2} \mathrm{C}$ address.


Figure 6. ADP1046A Address of 50h in the GUI
6. If the software does not detect the device, it enters into simulation mode. Ensure that the connecter is connected to the daughter card. Click the Scan for ADP1046A Now icon located on the top right hand corner of the screen, as shown in Figure 7.

7. Click the Load Board Settings icon (see Figure 7) and select the ADP1046A_FBPS_600W_xxxx.46b file. This file contains all the board information, including values of shunt and voltage dividers. Note that all board setting files have a .46b file extension.
8. The IC on the board comes preprogrammed, and this step is optional. The original register configuration is stored in the ADP1046A_FBPS_600W_xxxx.46r register file (note that all register files have a $\mathbf{4 6 r}$ file extension). The file can be loaded using the second icon from the left in Figure 8.
9. Connect a dc power source ( 385 V dc nominal, current limit to approximately 2 A ) and an electronic load at the output set to 1 A .
10. Connect a voltmeter on test points TP26(+) and TP46(-). Ensure that differential probes are used and that the ground of the probes are isolated if oscilloscope measurements are made on the primary side of the transformer.
11. Click the Dashboard Settings icon (see Figure 7) and turn on the software PS_ON.
12. The board is running and ready for evaluation. The output now reads 12 V dc.
13. Click the Monitor tab and then click the Flags and readings icon. This window provides a snapshot of the entire state of the PSU in a single user friendly window.


Figure 8. Different Icons on Dashboard for Loading and Saving .46r and .46b Files

## BOARD SETTINGS

Figure 9 shows the board settings.


Figure 9. Main Setup Window of ADP1046A GUI

## THEORY OF OPERATION DURING STARTUP

The following steps briefly describe the startup procedure of the ADP1046A, the power supply, and the operation of the state machine for the preprogrammed set of registers that are included in the design kit.

1. The on-board auxiliary power starts up at approximately 50 V dc . The on-board auxiliary power provides a drive voltage on the isolated side to an $\mathrm{LDO}(3.3 \mathrm{~V})$ that powers up the ADP1046A. After VDD ( 3.3 V ) is applied to the ADP1046A, it takes approximately $20 \mu$ s to $50 \mu$ s for VCORE to reach 2.5 V . The digital core is now activated, and the contents of the registers are downloaded in the EEPROM. The ADP1046A is now ready for operation.
2. PS_ON is applied. The power supply begins the programmed soft start ramp of 50 ms (programmable).
3. Because the soft start from precharge setting is active, the output voltage is sensed before the soft start ramp begins. Depending on the output voltage level, the effective soft start ramp is reduced by the proportional amount.
4. The PSU now is running in steady state. PGOOD1 turns on after the programmed debounce.
5. If a fault is activated during the soft start or steady state, the corresponding flag is set, and the programmed action is taken, such as Disable Power Supply and Re-enable after 1 s , Disable SR and OrFET, or Disable OUTAUX (see Figure 10).

## FLAGS SETTINGS CONFIGURATIONS

When a flag is triggered, the ADP1046A state machine waits for a programmable debounce time before taking any action. The response to each flag can be programmed individually. The flags can be programmed in a single window by selecting the Flag Settings icon under the Monitor tab in the GUI. This monitor window shows all the fault flags (if any) and the readings in one page. The Get First Flag button determines the first flag that was set in the case of a fault event.


Figure 10. Fault Configurations

## PWM SETTINGS

The ADP1046A has a fully programmable PWM setup that controls seven PWMs. Due to this flexibility, the IC can function in several different topologies, such as any isolated buck derived topology, push-pull, and flyback, and also has the control law for resonant converters.

Each PWM edge can be moved in 5 ns steps to achieve the appropriate dead time required, and the maximum modulation limit sets the maximum duty cycle.



Figure 11. PWM Settings Window in the GUI

Table 4. PWMs and Their Corresponding Switching Element

| PWM | Switching Element Being Controlled |
| :--- | :--- |
| OUTA to OUTD | Primary switch PWM configured for phase shifted topology |
| SR1, SR2 | Synchronous rectifier PWMs |
| OUTAUX | Not applicable |

## BOARD EVALUATION AND TEST DATA

## STARTUP



Figure 12. Startup at 340 V dc, 600 W Load (Software PS_ON) Green Trace: Output Voltage, $10 \mathrm{~V} / \mathrm{div}, 10 \mathrm{~ms} / \mathrm{div}$ Yellow Trace: Load Current, 2 A/div, $10 \mathrm{~ms} / \mathrm{div}$ Red Trace: Input Voltage, $50 \mathrm{~V} /$ div, $10 \mathrm{~ms} / \mathrm{div}$


Figure 13. Startup at 385 V dc, 600 W Load (Software PS_ON) Green Trace: Output Voltage, $10 \mathrm{~V} / \mathrm{div}, 10 \mathrm{~ms} / \mathrm{div}$ Yellow Trace: Load Current, 2 A/div, $10 \mathrm{~ms} / \mathrm{div}$ Red Trace: Input Voltage, $50 \mathrm{~V} /$ div, $10 \mathrm{~ms} / \mathrm{div}$


Figure 14. Startup at 385 V dc, Full Load Green Trace: Output Voltage, $10 \mathrm{~V} / \mathrm{div}, 10 \mathrm{~ms} / \mathrm{div}$ Yellow Trace: Primary Current, $2 \mathrm{~A} / \mathrm{div}, 10 \mathrm{~ms} / \mathrm{div}$


Figure 15. Primary Current at Full Load
Red Trace: Resonant Inductor Current, 1 A/div, $2 \mu \mathrm{~s} /$ div Yellow Trace: Primary Current, 1 A/div, $2 \mu \mathrm{~s} / \mathrm{div}$

OVERCURRENT AND SHORT-CIRCUIT PROTECTION


Figure 16. OCP at $385 \mathrm{~V} \mathrm{dc}, 15$ A Load (Action to Shutdown After $\sim 10 \mathrm{~ms}$ ) Green Trace: Output Voltage, $10 \mathrm{~V} / \mathrm{div}, 5 \mathrm{~ms} / \mathrm{div}$ Yellow Trace: Load Current, 5 A/div, 5 ms/div Red Trace: Input Voltage, $50 \mathrm{~V} / \mathrm{div}, 5 \mathrm{~ms} / \mathrm{div}$


Figure 17. OCP at $350 \mathrm{~V} \mathrm{dc}, 15$ A Load (Action to Shutdown After $\sim 10 \mathrm{~ms}$ ) Green Trace: Output Voltage, $10 \mathrm{~V} / \mathrm{div}, 5 \mathrm{~ms} / \mathrm{div}$ Yellow Trace: Load Current, 5 A/div, 5 ms/div Red Trace: Input Voltage, $50 \mathrm{~V} / \mathrm{div}, 5 \mathrm{~ms} / \mathrm{div}$


Figure 18. OCP at 385 V dc, 600 W to Output Shorted Red Trace: SR Drive, $5 \mathrm{~V} /$ div, $5 \mathrm{~ms} /$ div Green Trace: Output Voltage, 10 V/div, 200 us/div Yellow Trace: Output Current, 5 A/div


Figure 19. OCP, Hiccup Mode, 385 V dc, 600 W to Output Shorted Red Trace: SR Drive, $5 \mathrm{~V} /$ div, $5 \mathrm{~ms} /$ div Green Trace: Output Voltage, $10 \mathrm{~V} / \mathrm{div}, 200 \mu \mathrm{~s} / \mathrm{div}$ Yellow Trace: Output Current, 5 A/div

## PRIMARY GATE DRIVER DEAD TIME



Figure 20. Primary Gate Drive Voltage at Maximum Modulation (Output of iCoupler), $5 \mathrm{~V} / \mathrm{div}, 1 \mu \mathrm{~s} / \mathrm{div}$ Yellow Trace: OUTA, Red Trace: OUTB, Blue Trace: OUTC, Green Trace: OUTD


Figure 21. Primary Gate Drive Voltage at Maximum Modulation (Output of iCoupler) Showing Dead Time, Zoom In, 5 V/div, $0.2 \mu \mathrm{~s} / \mathrm{div}$ Yellow Trace: OUTA, Red Trace: OUTB, Blue Trace: OUTC, Green Trace: OUTD


Figure 22. Primary Gate Drive Voltage at Maximum Modulation (Output of iCoupler) Showing Dead Time, Zoom In, $5 \mathrm{~V} / \mathrm{div}, 0.2 \mu \mathrm{~s} / \mathrm{div}$ Yellow Trace: OUTA, Red Trace: OUTB, Blue Trace: OUTC, Green Trace: OUTD


Figure 23. Primary Gate Drive Voltage at Minimum Modulation (Output of iCoupler), $5 \mathrm{~V} / \mathrm{div}, 1 \mu \mathrm{~s} / \mathrm{div}$
Yellow Trace: OUTA, Red Trace: OUTB, Blue Trace: OUTC, Green Trace: OUTD


Figure 24. Primary Gate Drive Voltage at Minimum Modulation (Output of iCoupler) Showing Dead Time, Zoom In, 5 V/div, $0.2 \mu \mathrm{~s} / \mathrm{div}$ Yellow Trace: OUTA, Red Trace: OUTB, Blue Trace: OUTC, Green Trace: OUTD


Figure 25. Primary Gate Drive Voltage at Minimum Modulation
(Output of iCoupler) Showing Dead Time, Zoom In, 5 V/div, $0.2 \mu \mathrm{~s} / \mathrm{div}$ Yellow Trace: OUTA, Red Trace: OUTB, Blue Trace: OUTC, Green Trace: OUTD

CS1 PIN VOLTAGE (PRIMARY CURRENT)


Figure 26. Primary Current at 385 V dc, 300 W Load, $2 \mu \mathrm{~s} /$ div Yellow Trace: Primary Current Half Effect Probe, 1 A/div Green Trace: CS1 Pin Voltage, 270 mV/div


Figure 27. Primary Current at 385 V dc, 600 W Load, $2 \mu \mathrm{~s} /$ div Yellow Trace: Primary Current Half Effect Probe, 1 A/div

Green Trace: CS1 Pin Voltage, 270 mV/div

SYNCHRONOUS RECTIFIER PEAK INVERSE VOLTAGE


Figure 28. Synchronous Rectifier MOSFET Peak Reverse Voltage at 600 W Load, $385 \mathrm{~V} \mathrm{dc}, 50 \mathrm{~V} / \mathrm{div}, 2 \mu \mathrm{~s} / \mathrm{div}$


Figure 29. Synchronous Rectifier MOSFET Peak Reverse Voltage at 600 W Load, $385 \mathrm{~V} \mathrm{dc}, 50 \mathrm{~V} / \mathrm{div}, 500 \mathrm{~ns} / \mathrm{div}$

## OUTPUT VOLTAGE RIPPLE




Figure 31. Output Voltage AC-Coupled, $385 \mathrm{~V} \mathrm{dc}, 12.5 \mathrm{~A}, 500 \mathrm{mV} / \mathrm{div}$,
2 ms/div, Low Frequency Component

TRANSIENT VOLTAGE AT 385 V dc (NOMINAL VOLTAGE)

Load Step of 15\% to 50\%


Figure 32. Output Voltage Transient, $500 \mu \mathrm{~s} / \mathrm{div}$ Yellow Trace: Load Current, 2 A/div
Green Trace: Output Voltage (AC-Coupled), $500 \mathrm{mV} / \mathrm{div}$


Figure 33. Output Voltage Transient, $500 \mu \mathrm{~s} / \mathrm{div}$ Yellow Trace: Load Current, 2 A/div
Green Trace: Output Voltage (AC-Coupled), $500 \mathrm{mV} / \mathrm{div}$

Load Step of 50\% to 100\%


Figure 34. Output Voltage Transient, $500 \mu \mathrm{~s} / \mathrm{div}$
Yellow Trace: Load Current, 2 A/div
Green Trace: Output Voltage (AC-Coupled), $500 \mathrm{mV} / \mathrm{div}$


Figure 35. Output Voltage Transient, $500 \mu \mathrm{~s} / \mathrm{div}$
Yellow Trace: Load Current, 2 A/div
Green Trace: Output Voltage (AC-Coupled), $500 \mathrm{mV} / \mathrm{div}$

Load Step of 0\% to 50\%


Figure 36. Output Voltage Transient, $500 \mu \mathrm{~s} / \mathrm{div}$ Yellow Trace: Load Current, 2 A/div
Green Trace: Output Voltage (AC-Coupled), $500 \mathrm{mV} / \mathrm{div}$


Figure 37. Output Voltage Transient, $500 \mu \mathrm{~s} / \mathrm{div}$ Yellow Trace: Load Current, 2 A/div Green Trace: Output Voltage (AC-Coupled), $500 \mathrm{mV} / \mathrm{div}$

HOLD UP TIME AND VOLTAGE DROPOUT


Figure 38. Minimum Input Voltage of $\sim 330$ V dc Before Output Regulation is Lost at $600 \mathrm{~W}, 10 \mathrm{~ms} / \mathrm{div}$
Red Trace: Input Voltage Step, 50 V/div
Green Trace: Output Voltage, $10 \mathrm{~V} / \mathrm{div}$


Figure 39. Hold Up Time of $\sim 10.781$ ms Before Output Voltage Reaches 36 V (Minimum Telecom Input) at 600 W, $100 \mu$ F Input Capacitor, $10 \mathrm{~ms} / \mathrm{div}$ Red Trace: Input Voltage Step, 50 V/div Green Trace: Output Voltage, 10 V/div

## LINE VOLTAGE FEEDFORWARD



Figure 40. Line Voltage Feedforward Disabled, 600 W Load Red Trace: Input Voltage Step, 350 V dc to 385 V dc, 50 V/div Green Trace: Output Voltage (AC-Coupled), 200 mV/div


Figure 41. Line Voltage Feedforward Enabled, 600 W Load Red Trace: Input Voltage Step, 350 V dc to 385 V dc, 50 V/div Green Trace: Output Voltage (AC-Coupled), 200 mV/div


Figure 42. Line Voltage Feedforward Disabled, 600 W Load Red Trace: Input Voltage Step, 350 V dc to 385 V dc, 50 V/div Green Trace: Output Voltage (AC-Coupled), 200 mV/div


Figure 43. Line Voltage Feedforward Enabled, 600 W Load Red Trace: Input Voltage Step, 350 V dc to 385 V dc, 50 V/div
Green Trace: Output Voltage (AC-Coupled), $200 \mathrm{mV} / \mathrm{div}$

## ZVS WAVEFORMS FOR QA (PASSIVE TO ACTIVE TRANSITION)



Figure 44. Resonant Transition at No Load, $100 \mathrm{~ns} / \mathrm{div}$
Red Trace: VDS of QA, $100 \mathrm{~V} / \mathrm{div}$
Yellow Trace: VGS of QA, 5 V/div


Figure 45. Resonant Transition at 48 W Load, $100 \mathrm{~ns} / \mathrm{div}$
Red Trace: VDS of QA, $100 \mathrm{~V} /$ div
Yellow Trace: VGS of QA, 5 V/div


Figure 46. Resonant Transition at 300 W Load, 100 ns/div Red Trace: VDS of QA, $100 \mathrm{~V} / \mathrm{div}$ Yellow Trace: VGS of QA, 5 V/div


Figure 47. Resonant Transition at 600 W Load, 100 ns/div Red Trace: VDS of QA, 100 V/div Yellow Trace: VGS of QA, 5 V/div

## ZVS WAVEFORMS FOR QB (PASSIVE TO ACTIVE TRANSITION)



Figure 48. Resonant Transition at No Load, $100 \mu \mathrm{~s} / \mathrm{div}$ Red Trace: VDS of QB, $100 \mathrm{~V} / \mathrm{div}$ Yellow Trace: VGS of QB, 5 V/div


Figure 49. Resonant Transition at 48 W Load, $100 \mu \mathrm{~s} / \mathrm{div}$ Red Trace: VDS of QB, $100 \mathrm{~V} / \mathrm{div}$ Yellow Trace: VGS of QB, $5 \mathrm{~V} / \mathrm{div}$


Figure 50. Resonant Transition at 300 W Load, $100 \mu \mathrm{~s} / \mathrm{div}$ Red Trace: VDS of QB, $100 \mathrm{~V} / \mathrm{div}$ Yellow Trace: VGS of QB, $5 \mathrm{~V} / \mathrm{div}$


Figure 51. Resonant Transition at 600 W Load, $100 \mu \mathrm{~s} / \mathrm{div}$ Red Trace: VDS of QB, $100 \mathrm{~V} / \mathrm{div}$ Yellow Trace: VGS of QB, 5 V/div

ZVS WAVEFORMS FOR QC (PASSIVE TO ACTIVE TRANSITION)


Figure 52. Resonant Transition at 300 W Load, $200 \mu \mathrm{~s} / \mathrm{div}$
Red Trace: VDS of QC, $100 \mathrm{~V} / \mathrm{div}$ Yellow Trace: VGS of QC, 5 V/div


Figure 53. Resonant Transition at 600 W Load, $200 \mu \mathrm{~s} / \mathrm{div}$ Red Trace: VDS of QC, 100 V/div Yellow Trace: VGS of QC, 5 V/div

ZVS WAVEFORMS FOR QD (PASSIVE TO ACTIVE TRANSITION)


Figure 54. Resonant Transition at 0 A Load, $100 \mu \mathrm{~s} / \mathrm{div}$ Red Trace: VDS of QD, $100 \mathrm{~V} /$ div Yellow Trace: VGS of QD, 5 V/div


Figure 55. Resonant Transition at 300 W Load, $100 \mu \mathrm{~s} / \mathrm{div}$ Red Trace: VDS of QD, $100 \mathrm{~V} /$ div Yellow Trace: VGS of QD, 5 V/div

## UG-734

## CLOSED LOOP FREQUENCY RESPONSE

A network analyzer (AP200) was used to test the bode plots of the system. A continuous noise signal of 300 mV was injected across the entire frequency range across a $10 \Omega$ resistor in series (R35)

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with the output voltage divider using an isolation transformer. The operating condition was 385 V dc input and a load condition of 600 W with a soaking time of 45 minutes.


Figure 56. Bode Plots, 385 V dc Input, 12.5 A Load, Blue Trace: Gain in dB, Red Trace: Phase in Degrees, Crossover Frequency $=3.15 \mathrm{kHz}$, Phase Margin $=115.2^{\circ}$


Figure 57. Efficiency vs. Load at 385 V dc, 45 Minute Soaking Time, with On-Board Airflow


Figure 58. Efficiency vs. Line Voltage at 600 W Load

## TRANSFORMER SPECIFICATIONS

Table 5. Transformer Specifications

| Parameter | Min | Typ Max | Unit | Notes |
| :--- | :--- | :--- | :--- | :--- |
| Core and Bobbin |  | 3.316 |  | PQ3535, Magnetics, Inc., material or equivalent |
| Primary Inductance |  | 4 | mH | Pin 1 to Pin 6 |
| Leakage Inductance |  | 4 | $\mu \mathrm{H}$ | Pin 1 to Pin 6 with all other windings shorted |
| Resonant Frequency | 850 |  | kHz | Pin 1 to Pin 6 with all other windings open |



Figure 59. Transformer Electrical Diagram


Figure 60. Transformer Construction Diagram

## THERMAL TEST DATA

A thermal snapshot of the evaluation board was taken after running at 600 W with a 45 minute soaking time.


Figure 61. Thermals, Complete Board


Figure 62. Thermals, Primary Clamp Diode


Figure 63. Thermals, Synchronous Rectifier


Figure 64. Thermals, Output Inductor


Figure 65. Thermals, Output Current Sense Resistor


Figure 66. Thermals, Transformer


Figure 67. Thermals, Resonant Inductor


Figure 69. Thermals, Transformer


Figure 68. Thermals, Primary MOSFET

## EVALUATION BOARD SCHEMATICS AND LAYOUT




Figure 71. Schematic, Main Power Train


Figure 72. Schematic, Miscellaneous


Figure 73. Schematic, ADP1046A Daughter Card


Figure 74. Top Side Placement of Components


Figure 75. Bottom Side Placement of Components


Figure 76. Layout Layer 1


Figure 77. Layout Layer 2


Figure 78. Layout Layer 3


Figure 79. Layout Layer 4

## DAUGHTER CARD PCB LAYOUT



Figure 80. PCB Assembly, Top


Figure 81. PCB Layout, Top Layer


Figure 82. PCB Layout, Layer 2


Figure 83. PCB Layout, Layer 3


Figure 84. PCB Layout, Bottom Layer


Figure 85. PCB Layout, Silkscreen Bottom

## REGISTER SETTINGS FILE (.46r) FOR GUI

Copy the contents below into a text file and rename it using a . 46 r file extension. Load this file in the GUI using the Load Register Settings option. Ensure that the last line of the .46r file does not have a carriage return.

| Reg $(8 h)=$ F3h - Fault Configuration Register 1 $\operatorname{Reg}(9 \mathrm{~h})=7 \mathrm{Dh}-$ Fault Configuration Register 2 | Reg(4Ch) = A8h - PWM 3 Negative Edge Setting <br> Reg(4Dh) $=5 \mathrm{~h}-\mathrm{PWM} 4$ Positive Edge Timing |
| :---: | :---: |
| $\operatorname{Reg}(\mathrm{Ah})=58 \mathrm{~h}$ - Fault Configuration Register 3 | Reg (4Eh) $=8 \mathrm{~h}-\mathrm{PWM} 4$ Positive Edge Setting |
| Reg(Bh) = 0h - Fault Configuration Register 4 | Reg(4Fh) = 38h - PWM 4 Negative Edge Timing |
| Reg(Ch) = 88h - Fault Configuration Register 5 | Reg(50h) = A8h - PWM 4 Negative Edge Setting |
| Reg(Dh) = 88h - Fault Configuration Register 6 | Reg(51h) = 3Dh - SR 1 Positive Edge Timing |
| Reg(Eh) = C5h - Flag Configuration | Reg(52h) = A9h - SR 1 Positive Edge Setting |
| Reg(Fh) $=22 \mathrm{~h}$ - Soft-Start Blank Fault Flags | Reg(53h) = 38h - SR 1 Negative Edge Timing |
| Reg(11h) = C0h - RTD Current Settings | Reg(54h) = 3h - SR 1 Negative Edge Setting |
| Reg(22h) = 5Bh - CS1 Accurate OCP Limit | Reg(55h) = 5h - SR 2 Positive Edge Timing |
| Reg(26h) = 4Fh - CS2 Accurate OCP Limit | Reg(56h) = A8h - SR 2 Positive Edge Setting |
| $\operatorname{Reg}(27 \mathrm{~h})=21 \mathrm{~h}-\mathrm{CS1} / \mathrm{CS} 2$ Settings | Reg(57h) $=0 \mathrm{~h}-\mathrm{SR} 2$ Negative Edge Timing |
| Reg(28h) = 23h - VS Balance Settings | Reg(58h) = 0h - SR 2 Negative Edge Setting |
| Reg(29h) = 0h - Share Bus Bandwidth | Reg(59h) = 0h - PWM AUX Positive Edge Timing |
| Reg(2Ah) = 13h - Share Bus Setting | Reg(5Ah) = 0h - PWM AUX Positive Edge Setting |
| Reg(2Ch) = E4h - PSON/Soft Stop Settings | Reg(5Bh) $=3 \mathrm{Fh}-\mathrm{PWM}$ AUX Negative Edge Timing |
| Reg(2Dh) = 7Eh - PGOOD Debounce and Pin | Reg(5Ch) $=50 \mathrm{~h}-\mathrm{PWM}$ AUX Negative Edge Setting |
| Polarity Setting | Reg(5Dh) $=80 \mathrm{~h}-\mathrm{PWM}$ and SR Pin Disable |
| Reg(2Eh) = E5h - Modulation Limit | Setting |
| Reg(2Fh) $=4 \mathrm{~h}-$ OTP Threshold | Reg(5Fh) = B7h - Soft Start and Slew Rate |
| $\operatorname{Reg}(30 \mathrm{~h})=53 \mathrm{~h}-\mathrm{OrFET}$ | Setting |
| Reg(31h) = A2h - VS3 Voltage Setting | Reg(60h) = 10h - Normal Mode Digital Filter LF Gain Setting |
| Reg(32h) = 23h - VS1 Overvoltage Limit | Reg(61h) = D8h - Normal Mode Digital Filter |
| Reg(33h) = 27h - VS2 / VS3 Overvoltage Limit | Zero Setting |
| Reg(34h) = 46h - VS1 Undervoltage Limit | Reg(62h) = C3h - Normal Mode Digital Filter |
| Reg(35h) = FFh - Line Impedance Limit | Pole Setting |
| $\operatorname{Reg}(36 \mathrm{~h})=10 \mathrm{~h}$ - Load Line Impedance | Reg(63h) = Ah - Normal Mode Digital Filter HF |
| Reg(37h) $=$ 5Dh - Fast OVP Comparator Settings | Gain Setting |
| Reg(3Bh) $=0 \mathrm{Oh}$ - Light Load Disable Setting | Reg(64h) = 4Eh - Light Load Digital Filter LF Gain Setting |
| Reg(3Fh) = 94h - OUTAUX Switching Frequency Setting | Reg(65h) = AAh - Light Load Digital Filter Zero Setting |
| Reg(40h) = 14h - PWM Switching Frequency Setting | Reg(66h) = 64h - Light Load Digital Filter Pole Setting |
| Reg(41h) $=38 \mathrm{~h}$ - PWM 1 Positive Edge Timing | Reg(67h) = 15h - Light Load Digital Filter HF |
| Reg(42h) = A1h - PWM 1 Positive Edge Setting | Gain Setting |
| Reg(43h) = 6Dh - PWM 1 Negative Edge Timing | Reg(68h) = 0h - Reserved |
| Reg(44h) = 60h - PWM 1 Negative Edge Setting | Reg(69h) = 0h - Reserved |
| Reg(45h) = 0h - PWM 2 Positive Edge Timing | Reg(6Ah) = 0h - Reserved |
| Reg(46h) = A1h - PWM 2 Positive Edge Setting | Reg(6Bh) = 0h - Reserved |
| Reg(47h) = 35h - PWM 2 Negative Edge Timing | Reg(6Ch) = 0h - Reserved |
| Reg(48h) = 80h - PWM 2 Negative Edge Setting | Reg(6Dh) = 0h - Reserved |
| Reg(49h) = 3Dh - PWM 3 Positive Edge Timing | Reg(6Eh) = 0h - Reserved |
| Reg(4Ah) = 8h - PWM 3 Positive Edge Setting | Reg(6Fh) = 0h - Reserved |
| Reg(4Bh) = 0h - PWM 3 Negative Edge Timing | Reg(70h) = 0h - Reserved |

```
Reg(71h) = 4Eh - Soft Start Digital Filter LF
Gain Setting
Reg(72h) = AAh - Soft Start Digital Filter
Zero Setting
Reg(73h) = 64h - Soft Start Digital Filter
Pole Setting
Reg(74h) = 15h - Soft Start Digital Filter HF
Gain Setting
Reg(75h) = 4h - Voltage Feed Forward Settings
Reg(76h) = 0h - Volt Second Balance OUTA/OUTB
Settings
```

```
Reg(77h) = 0h - Volt Second Balance OUTC/OUTD
```

Reg(77h) = 0h - Volt Second Balance OUTC/OUTD
Settings
Settings
Reg(78h) = 0h - Volt Second Balance SR1/SR2
Reg(78h) = 0h - Volt Second Balance SR1/SR2
Settings
Settings
Reg(79h) = 0h - SR Delay Offset
Reg(79h) = 0h - SR Delay Offset
Reg(7Ah) = Fh - Filter Transitions
Reg(7Ah) = Fh - Filter Transitions
Reg(7Bh) = 40h - PG00D1 Masking
Reg(7Bh) = 40h - PG00D1 Masking
Reg(7Ch) = FFh - PGOOD2 Masking
Reg(7Ch) = FFh - PGOOD2 Masking
Reg(7Dh) = Ch - Light Load Mode Threshold
Reg(7Dh) = Ch - Light Load Mode Threshold
Settings

```
Settings
```


## ADP1046A Evaluation Board User Guide

## BOARD SETTINGS FILE (.46b) FOR GUI

Copy the contents below into a text file and rename it using a.46b file extension. Load this file in the GUI using the Load Board Settings option. Ensure that the last line of the $\mathbf{. 4 6 b}$ file does not have a carriage return.

| Input Voltage $=385 \mathrm{~V}$ | Topology $=1$ ( $0=$ Full Bridge: $1=$ Half |
| :---: | :---: |
| N1 = 28 | Bridge: 2 = Two Switch Forward: 3 = |
| N1 - 28 | Interleaved Two Switch Forward: 4 = Active |
| $\mathrm{N} 2=5$ | Clamp Forward: $5=$ Resonant Mode: $6=$ |
| $\mathrm{R}(\mathrm{CS} 2)=2.5 \mathrm{mOhm}$ | Custom) |
| $\mathrm{I}($ load $)=12.5 \mathrm{~A}$ | Switches / Diodes = 0 (0 = Switches: 1 = Diodes) |
| $\mathrm{R} 1=46.4 \mathrm{KOhm}$ | Diodes) |
| R2 = 1 KOhm | High Side / Low Side Sense (CS2) = 0 (1 = High-Side: 0 = Low-Side Sense) |
| $\mathrm{C} 3=1 \mathrm{uF}$ | Second LC Stage $=1$ (1 = Yes: $0=$ No) |
| $\mathrm{C} 4=1 \mathrm{uF}$ | CS1 Input Type $=0(1=A C: 0=D C)$ |
| N1 (CS1) $=1$ | R3 = 0 KOhm |
| N2 (CS1) $=100$ | R4 = 0 KOhm |
| R (CS1) $=51$ 0hm | PWM Main $=0$ ( $0=$ OUTA: $1=$ OUTB: $2=$ OUTC: |
| ESR (L1) $=6 \mathrm{mOhm}$ | 3 OUTD: $4=$ SR1: 5 = SR2: $6=$ OUTAUX) |
| $\mathrm{LI}=4.7 \mathrm{uH}$ | $\mathrm{C} 5=0 \mathrm{uF}$ |
| $\mathrm{C1}=1000 \mathrm{uF}$ | $\mathrm{C} 6=0 \mathrm{uF}$ |
| ESR $(\mathrm{C1})=35 \mathrm{mOhm}$ | $\mathrm{R} 6=65 \mathrm{KOhm}$ |
| ESR (L2) $=0 \mathrm{mOhm}$ | $\mathrm{R} 7=1 \mathrm{KOhm}$ |
| $\mathrm{L} 2=0 \mathrm{uH}$ | $\mathrm{C} 7=0 \mathrm{uF}$ |
| $\mathrm{C} 2=0 \mathrm{uF}$ | $\mathrm{L} 3=33 \mathrm{uH}$ |
| ESR $(\mathrm{C} 2)=0 \mathrm{mOhm}$ | $\mathrm{Lm}=0 \mathrm{uH}$ |
| $R$ (Normal-Mode) (Load) $=3.84$ Ohm | ResF $=0 \mathrm{kHz}$ |
| R (Light-Load-Mode) (Load) = 24 0hm | $\mathrm{R} 8=0 \mathrm{mOhm}$ |
| Cap Across R1 \& R2 = 0 " $(1=$ Yes: $0=$ No)" | $\mathrm{R} 9=0 \mathrm{mOhm}$ |

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 6. ADP1046A Evaluation Board Bill of Materials

| Qty | Reference | Value | Description | Manufacturer | Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 3 | C1, C22, C74 | 1 nF | Cap, cer, 1000 pF, $50 \mathrm{~V}, 10 \%$, X7R, SMD | AVX Corp | 08055C102KAT2A |
| 1 | C11 | $330 \mu \mathrm{~F}$ | Cap, alum, $330 \mu \mathrm{~F}, 80 \mathrm{~V}, 20 \%$, SMD | Panasonic | EEV-FK1K331M |
| 6 | $\begin{aligned} & \text { C15, C16, C18, } \\ & \text { C20, C29, C31 } \end{aligned}$ | $1 \mu \mathrm{~F}$ | Cap, cer, $1.0 \mu \mathrm{~F}, 25 \mathrm{~V}, 10 \%$, X7R, SMD | TDK Corp | C2012X7R1E105K085AB |
| 4 | C17, C19, C21, C30 | $0.1 \mu \mathrm{~F}$ | Cap, cer, $0.1 \mu \mathrm{~F}, 25 \mathrm{~V}, 10 \%$, X7R, SMD | Vishay | VJ0805Y104KXXAC |
| 1 | C38 | Do not insert |  |  |  |
| 1 | C41 | $680 \mu \mathrm{~F}$ | Cap, alum, $680 \mu \mathrm{~F}, 63 \mathrm{~V}, 20 \%$, SMD | Panasonic | EEV-FK1J681M |
| 1 | C43 | Do not insert |  |  |  |
| 1 | C44 | $4.7 \mu \mathrm{~F}$ | Cap, cer, $4.7 \mu \mathrm{~F}, 25 \mathrm{~V}, 10 \%$, X7R, SMD | TDK Corp | C3225X7R1E475K |
| 1 | C47 | $1 \mu \mathrm{~F}$ | Cap, cer, $1 \mu \mathrm{~F}, 25 \mathrm{~V}, \pm 10 \%$, X7R | Digi-Key | 490-4785-1-ND |
| 4 | C60 to C63 | 33 pF | Cap, cer, $33 \mathrm{pF}, 50 \mathrm{~V}, \pm 5 \%$, NPO, SMD | AVX Corp | 08055A330JAT2A |
| 11 | $\begin{aligned} & \text { C68, C70, C73, C76 } \\ & \text { to C81, C83, C84 } \end{aligned}$ | $10 \mu \mathrm{~F}$ | Cap, ceramic, $10 \mu \mathrm{~F}, 63 \mathrm{~V}, \pm 10 \%$, X7R, SMD | Murata | KCM55QR71J106KH01K |
| 1 | C69 | 2200 pF | Cap, cer, 2200 pF, 500 V ac, $20 \%$, radial | Vishay/BC | VY1222M47Y5UQ63V0 |
| 2 | C71, C72 | $0.33 \mu \mathrm{~F}$ | Cap, film, $0.33 \mu \mathrm{~F}, 450 \mathrm{Vdc}$, radial | Panasonic-ECG | ECW-F2W334JAQ |
| 1 | C75 | $0.022 \mu \mathrm{~F}$ | Cap, film, $0.022 \mu \mathrm{~F}, 1.25 \mathrm{kV}$ dc, radial | EPCOS, Inc. | B32652A7223J |
| 1 | C82 | $0.1 \mu \mathrm{~F}$ | Cap, cer, $0.1 \mu \mathrm{~F}, 50 \mathrm{~V}, 10 \%$, X7R, SMD | Murata | GRM21BR71H104KA01L |
| 1 | C94 | 33 nF | Cap, cer, $0.33 \mu \mathrm{~F}, 200 \mathrm{~V}, 10 \%$, X7R, SMD | AVX Corp | 12062C333KAT2A |
| 1 | C106 | $100 \mu \mathrm{~F}$ | Cal, alum, $100 \mu \mathrm{~F}, 400 \mathrm{~V}, 20 \%$, snap | Panasonic-ECG | EET-HC2G101HA |
| 1 | C111 | $2.2 \mu \mathrm{~F}$ | Cap, ceramic, $0.033 \mu \mathrm{~F}, 100 \mathrm{~V}, 5 \%$, NPO, SMD | Kemet | C1812C333J1GACTU |
| 3 | C114 to C116 | $1 \mu \mathrm{~F}$ | Cap, $0.33 \mu \mathrm{~F}, 630 \mathrm{~V} \mathrm{dc}$, metal poly | TDK Corp | CKG57NX7T2J105M |
| 1 | C120 | $0.1 \mu \mathrm{~F}$ | Cap, ceramic, $0.1 \mu \mathrm{~F}, 100 \mathrm{~V}, 10 \%$, X7R SMD | AVX Corp | 12061C104KAT2A |
| 2 | D10, D11 | RS1J | SMD, diode, super fast, $200 \mathrm{~V}, 1 \mathrm{~A}$ | Vishay | RS1J-E3/61T |
| 2 | D13, D47 | 1N4148 | Diode, SML, sig, $100 \mathrm{~V}, 0.15$ A, SMD | Diodes, Inc. | 1N4148W-13-F |
| 1 | D19 | MMSZ5222BT1G | SMD diode Zener, $2.5 \mathrm{~V}, 500 \mathrm{~mW}$ | ON Semiconductor | SMAZ16-FDICT-ND |
| 1 | D20 | Do not insert |  |  |  |
| 2 | D36, D37 | S3J-E3/57T | Diode glass, passivated, $3 \mathrm{~A}, 600 \mathrm{~V}, \mathrm{SMB}$ | Vishay | S3J-E3/57T |
| 1 | D48 | MMBD4148CC | Diode array, $100 \mathrm{~V}, 200 \mathrm{~mA}$ | Fairchild | MMBD4148CC |
| 1 | D49 | Yellow | LED, yellow, clear, SMD | Visual | CMD15-21VYC/TR8 |
| 1 | D50 | MMBD4148CA | Diode array, $100 \mathrm{~V}, 200 \mathrm{~mA}$ | Fairchild | MMBD4148CA |
| 1 | D51 | Red | LED, high efficiency, red, clear, SMD | Visual | CMD15-21VRC/TR8 |
| 4 | D52 to D55 | 1N4148 | Diode switch, $100 \mathrm{~V}, 400 \mathrm{~mW}, \mathrm{SMD}$ | Diodes, Inc. | 1N4148W-7-F |
| 2 | D58, D59 | ES1D | Diode fast SW, $300 \mathrm{~V}, 1 \mathrm{~A}$, SMA | Fairchild | ES1F |
| 1 | D62 | 1N5819 | Diode Schottky, 40 V, 1 A, SMD | Diodes, Inc. | 1N5819HW-7-F |
| 2 | D63, D64 | MMBD4148SE | Diode array, $100 \mathrm{~V}, 200 \mathrm{~mA}$ | Fairchild | MMBD4148SE |
| 1 | F2 | 5A | Holder, PC fuse, 5 mm , low profile | Keystone | 4527 |
| 1 | J1 | BNC/R | Conn jack, vertical, PCMNT, gold | Emerson | 131-3701-261 |
| 1 | J8 | VIN+ | Conn jack banana, uninsulated, panel mount | Emerson | 108-0740-001 |
| 1 | J9 | VIN- | Conn jack banana, uninsulated, panel mount | Emerson | 108-0740-001 |
| 1 | J11 | VOUT+ | Conn jack banana, uninsulated, panel mount | Emerson | 108-0740-001 |
| 1 | J12 | VOUT- | Conn jack banana, uninsulated, panel mount | Emerson | 108-0740-001 |
| 1 | J15 | ADP1046_DC | Conn, heade, 30 pos, 100 vert, dual | TE Connectivity | 4-102973-0-15 |
| 1 | J16 | HDR1X4 | Conn, header, 4 pos, SGL, PCB, 30, gold | FCI | 69167-104HLF |
| 1 | J17 | HDR1X4 | Conn, female on BRD, 10 pos, vert T/H | TE Connectivity | 8-215079-0 |
| 1 | J18 | HDR1X4 | Conn, header, female, $16 \mathrm{PS}, 0.1$ " DL tin | Sullins Connector | PPTC082LFBN-RC |
| 1 | J28 | HDR1X2 | Conn, header, 2 pos, 0.100 vert tin | Molex, Inc. | 22232021 |
| 1 | L6 | CHOKE | Switchmode IND., $33 \mu \mathrm{H}$ | Precision | LSM-28285-0330 |
| 1 | L8 | $4.7 \mu \mathrm{H}$ | High current IHLP IND $4.7 \mu \mathrm{H}, 25 \mathrm{~A}$ | Vishay Dale | IHLP6767GZER4R7M01 |


| Qty | Reference | Value | Description | Manufacturer | Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 4 | QA to QD | SPP20N60CFD | MOSFET N-Ch, 650 V, 20.7 A | Infineon | SPP20N60CFD |
| 2 | Q9, Q22 | IPB107N20N3 G | MOSFET N-Ch, $200 \mathrm{~V}, 88 \mathrm{~A}$ | Infineon | IPB107N20N3 G |
| 1 | Q10 | MMBT3904 | Trans, GP, NPN, $200 \mathrm{~mA}, 40 \mathrm{~V}$ | Fairchild | MMBT3904 |
| 1 | Q21 | BSS138 | MOSFET N-Ch, $100 \mathrm{~V}, 170 \mathrm{~mA}$, SMD | Diodes, Inc. | BSS123-7-F |
| 1 | Q23 | BSZ22DN20NS3 G | MOSFET N-Ch, $200 \mathrm{~V}, 7 \mathrm{~A}$ | Infineon | BSZ22DN20NS3 G |
| 1 | RTD | $100 \mathrm{k} \Omega$ | Thermister, NTC, $100 \mathrm{k} \Omega, \pm 1 \%$, SMD | Murata | NCP15WF104F03RC |
| 1 | R2 | 0.002 | Res, $0.002 \Omega, 2 \mathrm{~W}, 1 \%$, SMD | Stackpole Electronics | CSNL2512FT2L00 |
| 4 | R25, R34, R65, R68 | $10 \mathrm{k} \Omega$ | Res, $10.0 \mathrm{k} \Omega, 1 / 2 \mathrm{~W}, \mathrm{SMD}$ | Vishay | CRCW120610KOFKEAHP |
| 2 | R40, R93 | $2.2 \mathrm{k} \Omega$ | Res, $2.20 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$, SMD | Yageo | RC0805FR-072K2L |
| 4 | R42, R43, R45, R49 | 0 | Res, $0 \Omega, 1 / 8 \mathrm{~W}, 1 \%$, SMD | Vishay Dale | CRCW08050000Z0EA |
| 6 | $\begin{aligned} & \text { R44, R64, R71, } \\ & \text { R74, R75, R78 } \end{aligned}$ | 0 | Res, $0.0 \Omega, 1 / 8 \mathrm{~W}, 5 \%$, SMD | Yageo | RC0805JR-070RL |
| 6 | $\begin{aligned} & \text { R51, R118 to } \\ & \text { R121, R123 } \end{aligned}$ | Short pin | Short pin |  |  |
| 1 | R52 | $22 \mathrm{k} \Omega$ | Res, $22.0 \mathrm{k} \Omega, 3 / 4 \mathrm{~W}, 5 \%$, SMD | Vishay Dale | CRCW201022KOJNEF |
| 1 | R59 | 200 | Res, $200 \Omega, 1 / 8 \mathrm{~W}, 5 \%$, SMD | Yageo | RC0805JR-07200RL |
| 1 | R66 | Do not insert |  |  |  |
| 1 | R70 | $16.5 \mathrm{k} \Omega$ | Res, $16.5 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$, SMD | Yageo | RC0805FR-0716K5L |
| 2 | R73, R116 | 0 | SMD res, 0 ת, 3/4 W, 5\% | Vishay Dale | 311-1.00CRCT-ND |
| 1 | R76 | 10 | Res, $10.0 \Omega, 1 / 8 \mathrm{~W}, 5 \%$, SMD | Yageo | RC0805JR-0710RL |
| 1 | R77, R79 | Do not insert |  |  |  |
| 3 | R87, R95, R96 | 100 | Res, $100 \Omega, 1 / 8 \mathrm{~W}, 1 \%$, SMD | Yageo | 311-100CRCT-ND |
| 2 | R109, R111 | 1 | Res, $1.0 \Omega, 3 / 4 \mathrm{~W}, 5 \%$, SMD | Vishay Dale | CRCW20101R00JNEF |
| 4 | R112 to R115 | $91 \mathrm{k} \Omega$ | Res, $91.0 \mathrm{k} \Omega, 2 \mathrm{~W}, 1 \%$, SMD | TE Connectivity | 352191 KFT |
| 1 | R117 | 0 | SMD, res, $0.0 \Omega, 1 / 8 \mathrm{~W}, 5 \%$ | Digi-Key | 311-0.0ARCT-ND |
| 1 | R122 | $10 \mathrm{k} \Omega$ | Res, $10.0 \mathrm{k} \Omega, 1 / 2 \mathrm{~W}, 1 \%$, SMD | Stackpole | RNCP1206FTD10K0 |
| 2 | R128, R129 | 4.99 | Res, 4.99 , 1/8 W, 1\%, SMD | Vishay Dale | CRCW08054R99FKEA |
| 4 | R130 to R133 | 2 | Res, $2.0 \Omega, 1 / 2 \mathrm{~W}, 1 \%$, SMD | Susumu | RL1632R-2R00-F |
| 1 | SW2 |  | SW slide SPDT, $30 \mathrm{~V}, 0.2 \mathrm{~A}, \mathrm{PC}$ mount | E-Switch | EG1218 |
| 6 | TP4, TP 12 to TP16 |  | Test point, PC, multipurpose, red | Keystone Electronics | 5010 |
| 11 | TP23,TP26, TP27, TP39, TP41, TP46 to TP50, TP52 |  | Test point, PC, mini, .040 " D , red | Keystone Electronics | 5010 |
| 1 | T5 |  | XFRMR, current sense, $37 \mathrm{~A}, 20 \mathrm{mH}, \mathrm{T} / \mathrm{H}$ | Pulse | PE-67100NL |
| 1 | T12 | PQ3535 | Transformer full bridge, 600 W | Precision, Inc. | 019-7365-00R |
| 1 | U7 | ADP3654 | High speed, dual, 4 A MOSFET driver | Analog Devices, Inc. | ADP3654ARDZ |
| 2 | U17, U18 | ADuM4223 | Digital isolated precision half-bridge driver | Analog Devices, Inc. | ADuM4223ARWZ |

Table 7. ADP1046A Daughter Card Bill of Materials

| Qty. | Reference | Value | Description | Manufacturer | Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | C5 | 1.0 FF | Cap, cer, $1.0 \mu \mathrm{~F}, 50 \mathrm{~V}, 10 \%$, X7R | Murata | GRM32RR71H105KA01L |
| 1 | C6 | 330 pF | Cap, cer, $330 \mathrm{pF}, 10 \%, 100 \mathrm{~V}, \mathrm{X} 7 \mathrm{R}$ | AVX | 08051C331KAT2A |
| 3 | C8, C11, C14 | $0.1 \mu \mathrm{~F}$ | Cap, cer, $0.1 \mu \mathrm{~F}, 10 \%, 50 \mathrm{~V}, \mathrm{X7R}$ | AVX | 08055C104KAT2A |
| 2 | C10, C13 | 100 pF | Cap, cer, $0.00 \mu \mathrm{~F}, 10 \%, 100 \mathrm{~V}, \mathrm{X} 7 \mathrm{R}$ | AVX | 08055C101KAT2A |
| 1 | C12 | 4.7 \% | Cap, cer, $4.7 \mu \mathrm{~F},+/-10 \%, 10 \mathrm{~V}, \mathrm{X} 7 \mathrm{R}$ | TY | LMK212B7475KG-T |
| 1 | C15 | 1000 pF | Cap, cer, 1000 pF, 10\%, 100 V, X7R | TDK | C2012X7R1A475M |
| 2 | D1, D2 | 1N4148 | Diode SW, 150 mA , 100 V | Micro Commercial | 1N4448W-TP |
| 1 | D6 | LED | LED, super red clear, $75 \mathrm{~mA}, 1.7 \mathrm{~V}$, SMD | Chicago Lighting | CMD15-21SRC/TR8 |
| 1 | J1 | CON30 | Conn, header, female, 30PS, 0.1" DL tin | Sullins Connector | PPTC152LFBN-RC |
| 1 | J7 | HEADER4X1 | Conn, header, 4 pos, SGL PCB 30 gold | FCl | 69167-104HLF |
| 1 | R1 | $65 \mathrm{k} \Omega$ | Res, $65 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$, SMD | Any | Any |
| 1 | R2 | $1 \mathrm{k} \Omega$ | Res, $1.00 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$, SMD | Any | Any |
| 2 | R3, R4 | $4.99 \mathrm{k} \Omega$ | Res, $4.99 \mathrm{k} \Omega, 1 / 10 \mathrm{~W}, 0.1 \%, \pm 25 \mathrm{ppm}$, SMD | Any | Any |
| 3 | R5, R7, R10 | $46.4 \mathrm{k} \Omega$ | Res, $11.0 \mathrm{k} \Omega, 1 / 10 \mathrm{~W}, 1 \%, \pm 25 \mathrm{ppm}$, SMD | Any | Any |
| 3 | R6, R8, R11 | $1 \mathrm{k} \Omega$ | Res, $1.00 \mathrm{k} \Omega, 1 / 10 \mathrm{~W}, 1 \%, \pm 25 \mathrm{ppm}$, SMD | Any | Any |
| 1 | R13 | $0 \Omega$ | Res, $0.0 \Omega, 1 / 8 \mathrm{~W}, 5 \%$, SMD | Any | Any |
| 6 | $\begin{aligned} & \text { R14, R15, R24, } \\ & \text { R29, R32, R33 } \end{aligned}$ | $2.2 \mathrm{k} \Omega$ | Res, $2.20 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, \mathrm{SMD}$ | Any | Any |
| 2 | R19, R20 | $10 \mathrm{k} \Omega$ | Res, $10 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 0.1 \%$, SMD | Any | Any |
| 1 | R21 | $5.1 \mathrm{k} \Omega$ | Res, $5.10 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}$, SMD | Any | Any |
| 1 | U1 | ADP1046A | Secondary side power supply controller | Analog Devices, Inc. | ADP1046A |
| 1 | U2 | ADP3303 | IC, LDO linear regulator, $200 \mathrm{~mA}, 3.3 \mathrm{~V}$ | Analog Devices, Inc. | ADP3303AR-3.3-ND |
| 9 | $\begin{aligned} & \mathrm{C} 1 \text { to } \mathrm{C}, \mathrm{C}, \mathrm{C}, \mathrm{C}, \\ & \mathrm{C} 16 \text { to } \mathrm{C} 18 \\ & \hline \end{aligned}$ | Do not insert |  |  |  |

$1^{2} \mathrm{C}$ refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).


ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## Legal Terms and Conditions





















 submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

