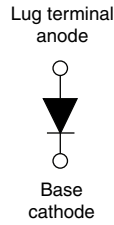


# High Performance Schottky Rectifier, 120 A


**HALF-PAK (D-67)**

**FEATURES**

- 175 °C T<sub>J</sub> operation
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Designed and qualified for industrial level
- UL approved file E222165
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS  
COMPLIANT**
**PRODUCT SUMMARY**

I <sub>F(AV)</sub>	120 A
V <sub>R</sub>	45 V
Package	HALF-PAK (D-67)
Circuit	Single diode

**DESCRIPTION**

The VS-121NQ.. high current Schottky rectifier module series has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

**MAJOR RATINGS AND CHARACTERISTICS**

SYMBOL	CHARACTERISTICS	VALUES	UNITS
I <sub>F(AV)</sub>	Rectangular waveform	120	A
V <sub>R(RRM)</sub>		45	V
I <sub>F(SM)</sub>	t <sub>p</sub> = 5 μs sine	16 000	A
V <sub>F</sub>	120 A <sub>pk</sub> , T <sub>J</sub> = 125 °C	0.6	V
T <sub>J</sub>	Range	-55 to +175	°C

**VOLTAGE RATINGS**

PARAMETER	SYMBOL	VS-121NQ045PbF	UNITS
Maximum DC reverse voltage	V <sub>R</sub>	45	V
Maximum working peak reverse voltage	V <sub>RWM</sub>		

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current See fig. 5	I <sub>F(AV)</sub>	50 % duty cycle at T <sub>C</sub> = 137 °C, rectangular waveform	120	A
Maximum peak one cycle non-repetitive surge current See fig. 7	I <sub>F(SM)</sub>	5 μs sine or 3 μs rect. pulse	16 000	A
		10 ms sine or 6 ms rect. pulse	2000	
Non-repetitive avalanche energy	E <sub>AS</sub>	T <sub>J</sub> = 25 °C, I <sub>AS</sub> = 13 A, L = 1 mH	81	mJ
Repetitive avalanche current	I <sub>AR</sub>	Current decaying linearly to zero in 1 μs Frequency limited by T <sub>J</sub> maximum V <sub>A</sub> = 1.5 x V <sub>R</sub> typical	13	A



ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop See fig. 1	$V_{FM}^{(1)}$	120 A	$T_J = 25\text{ }^\circ\text{C}$	0.65	V
		240 A		0.82	
		120 A	$T_J = 125\text{ }^\circ\text{C}$	0.6	
		240 A		0.76	
Maximum reverse leakage current See fig. 2	$I_{RM}$	$T_J = 25\text{ }^\circ\text{C}$	$V_R = \text{Rated } V_R$	10	mA
		$T_J = 125\text{ }^\circ\text{C}$		90	
Maximum junction capacitance	$C_T$	$V_R = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz) $25\text{ }^\circ\text{C}$		5200	pF
Typical series inductance	$L_S$	From top of terminal hole to mounting plane		7.0	nH
Maximum voltage rate of change	dV/dt	Rated $V_R$		10 000	V/ $\mu\text{s}$

**Note**

(1) Pulse width = 500  $\mu\text{s}$

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Maximum junction and storage temperature range	$T_J, T_{Stg}$		-55 to 175	$^\circ\text{C}$		
Maximum thermal resistance, junction to case	$R_{thJC}$	DC operation See fig. 4	0.38	$^\circ\text{C/W}$		
Typical thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, smooth and greased	0.05			
Approximate weight			30	g		
			1.06	oz.		
Mounting torque	minimum	Non-lubricated threads	3 (26.5)	N · m (lbf · in)		
	maximum		4 (35.4)			
Terminal torque	minimum		3.4 (30)			
	maximum		5 (44.2)			
Case style					HALF-PAK module	

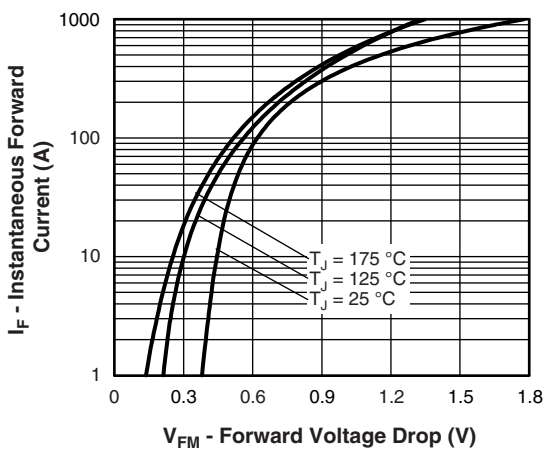


Fig. 1 - Maximum Forward Voltage Drop Characteristics

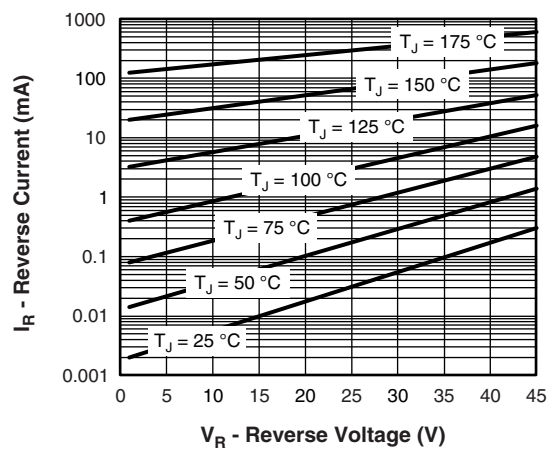


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

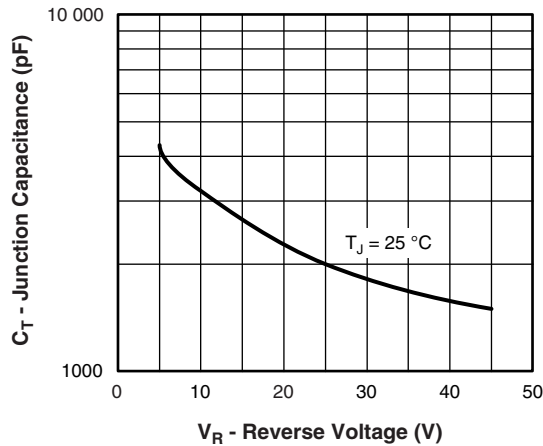


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

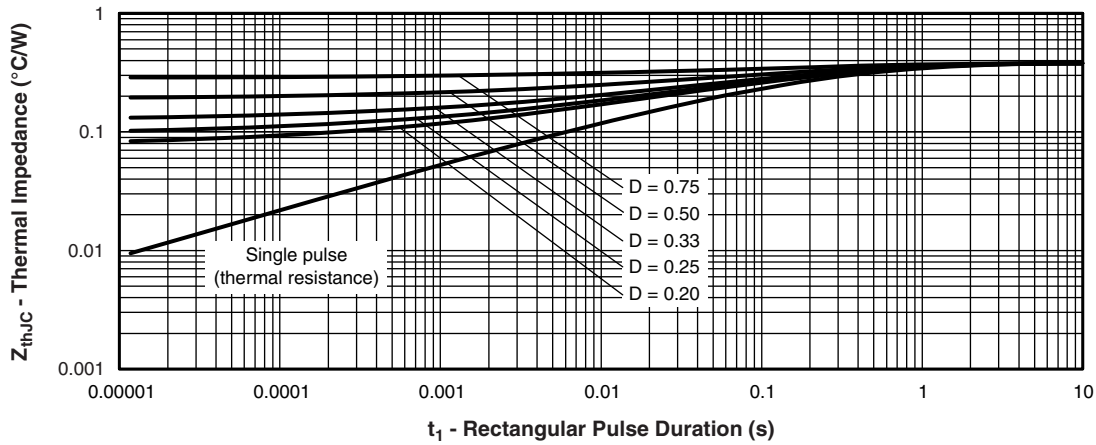


Fig. 4 - Maximum Thermal Impedance  $Z_{thJC}$  Characteristics

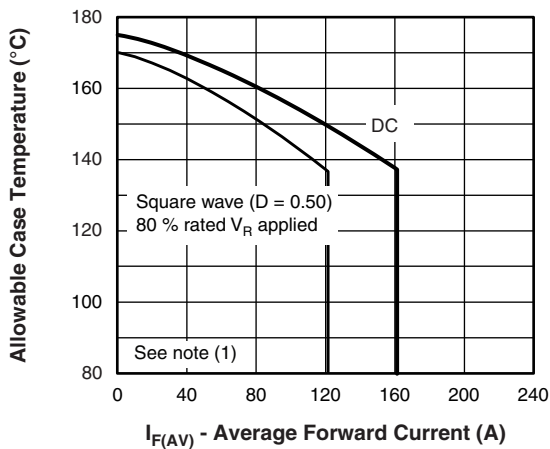


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

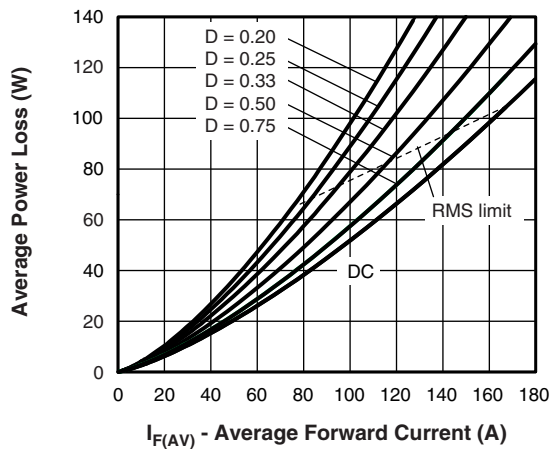


Fig. 6 - Forward Power Loss Characteristics

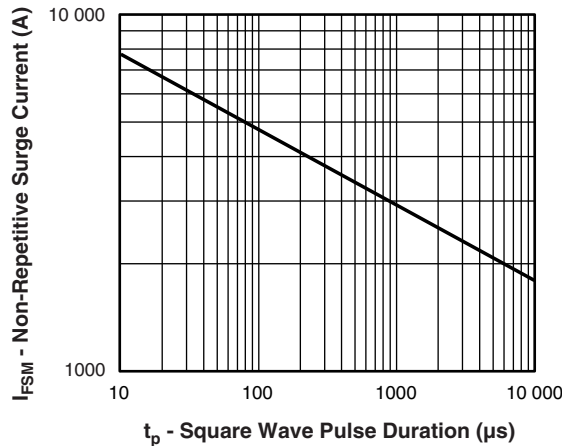


Fig. 7 - Maximum Non-Repetitive Surge Current

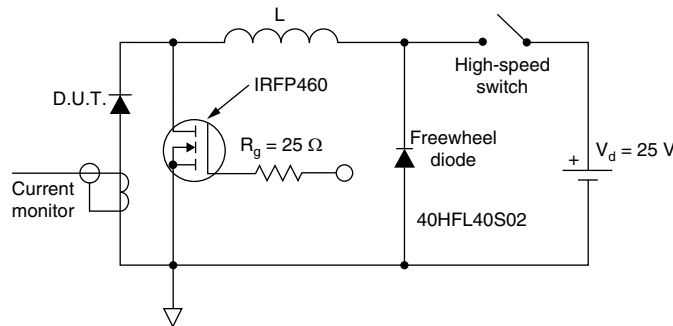


Fig. 8 - Unclamped Inductive Test Circuit

**Note**

- (1) Formula used:  $T_C = T_J - (P_d + P_{d_{REV}}) \times R_{thJC}$ ;
- $P_d$  = Forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 6);
- $P_{d_{REV}}$  = Inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R$  at  $V_{R1}$  = Rated  $V_R$

**ORDERING INFORMATION TABLE**

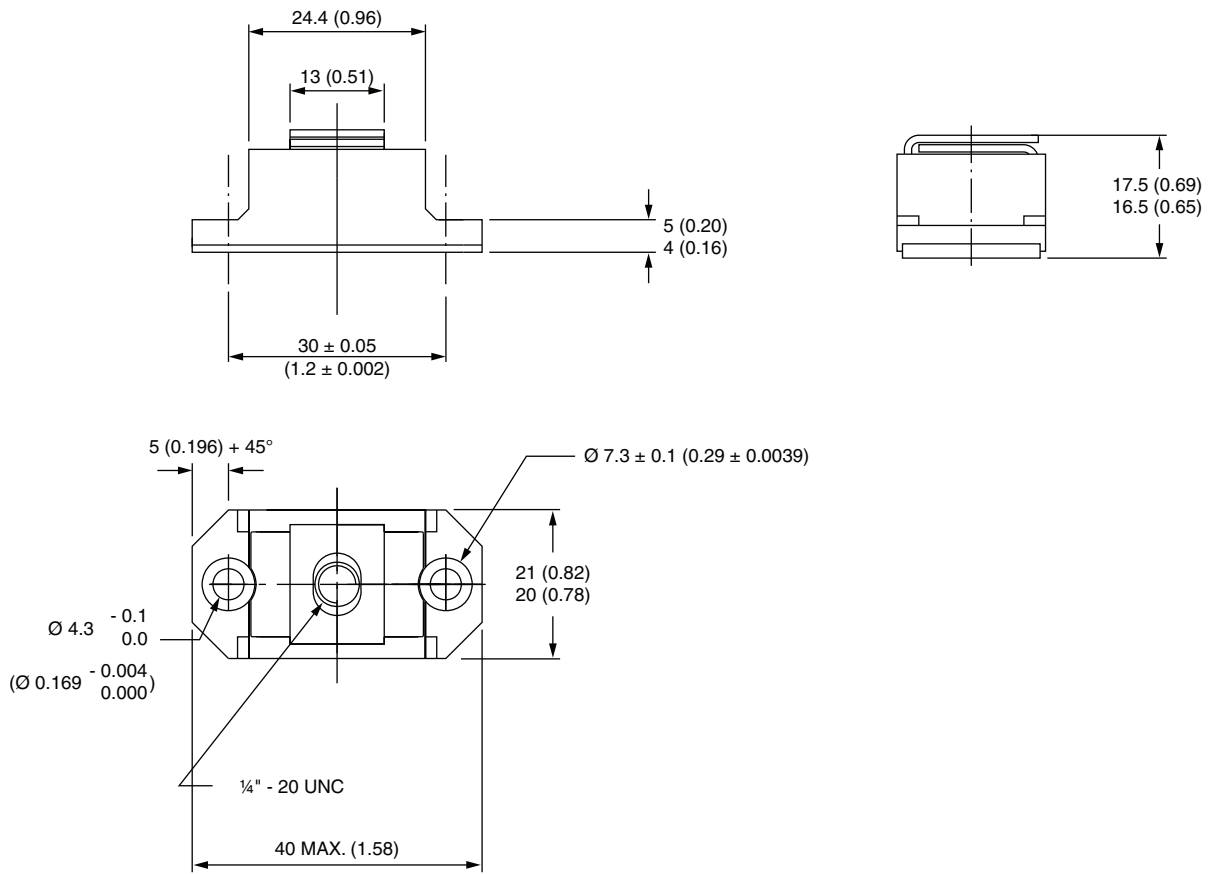
Device code	<b>VS-</b>	<b>12</b>	<b>1</b>	<b>N</b>	<b>Q</b>	<b>045</b>	<b>PbF</b>
	①	②	③	④	⑤	⑥	⑦

- 1** - Vishay Semiconductors product
- 2** - Average current rating (x 10)
- 3** - Product silicon identification
- 4** - N = Not isolated
- 5** - Q = Schottky rectifier diode
- 6** - Voltage rating (045 = 45 V)
- 7** - Lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95020">www.vishay.com/doc?95020</a>

## D-67 HALF-PAK

**DIMENSIONS** in millimeters (inches)





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